CLAIMS

What is claimed is:

1. A method comprising:

determining processor utilization in a data processing system; and

synchronizing execution of a plurality of threads in the data processing system to prevent interrupting the determining of the processor utilization.

2. The method of claim 1, further including processing the plurality of threads simultaneously on a plurality of logical processors.

3. The method of claim 2, the determining including one of the plurality of logical processors determining the processor utilization.

4. The method of claim 3, wherein the synchronizing further includes executing a predetermined unit of code on the plurality of logical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization.

5. The method of claim 4, wherein determining the processor utilization comprises calculating a frequency of the one of the plurality of logical processors.

6. The method of claim 1, further including processing the plurality of threads simultaneously on a plurality of physical processors.

7. The method of claim 6, wherein the determining includes one of the plurality of physical processors determining the processor utilization.

8. The method of claim 7, wherein synchronizing the execution of the plurality of threads comprises

executing a predetermined unit of code on the plurality of physical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization.

9. The method of claim 8, wherein determining the processor utilization comprises calculating a frequency of the one of the plurality of physical processors.

10. A method comprising:

determining processor utilization in a system executing at least a first thread and a second thread; and

pausing execution of the second thread during the determining of the processor utilization.

11. The method of claim 10, further comprising executing at least the first and the second threads simultaneously on at least a first processor and a second processor in the system.

12. The method of claim 10, the determining including the first processor determining the processor utilization.

13. An apparatus comprising:

a plurality of processors, one of the plurality of processors to determine processor utilization and the remaining processors to execute a predetermined unit of code to prevent interrupting the one determining the processor utilization; and

a bus coupling the plurality of processors to each other.

14. The apparatus of 13, further comprising a performance monitor counter coupled to each of the plurality of processors to keep track of when the processor is active.

15. The apparatus of 14, the performance monitor counter to provide a count for determining the processor utilization.

16. The apparatus of claim 13, wherein the plurality of processors comprise a plurality of logical processors to execute threads simultaneously.

17. The apparatus of claim 13, wherein execution of the predetermined unit of code causes the remaining processors to pause.

18. A machine-accessible medium that provides instructions that, if executed by a processor, will cause the processor to perform operations comprising:

determining processor utilization; and

synchronizing execution of a plurality of threads to prevent interrupting the determining of the processor utilization.

19. The machine-accessible medium of claim 18, wherein the operations further comprise processing the plurality of threads simultaneously on a plurality of logical processors.

20. The machine-accessible medium of claim 18, wherein the determining includes calculating a frequency of the processor.

21. A system comprising:

a plurality of dynamic random access memory (DRAM) devices; and

a processing device, coupled to the plurality of DRAM devices, operable to perform operations comprising:

determining processor utilization; and

synchronizing execution of a plurality of threads to prevent interrupting the determining of the processor utilization.

22. The system of claim 21, wherein the operations further include processing the plurality of threads simultaneously with a plurality of logical processors.

23. The system of claim 22, wherein the determining includes one of the plurality of logical processors determining the processor utilization.

24. The system of claim 23, wherein the synchronizing further includes executing a predetermined unit of code on the plurality of logical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization.

25. The system of claim 21, wherein the operations further comprise processing the plurality of threads with a plurality of physical processors.

26. The system of claim 25, wherein the processing of the plurality of threads includes one of the plurality of physical processors determining the processor utilization.

27. The system of claim 26, wherein the synchronizing further includes executing a predetermined unit of code on the plurality of physical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization.